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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,943	03/01/2002	Kazuya Kawakami	843.41231X00	8260

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EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,943	KAWAKAMI ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *14-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunter (U. S. Pat. 6,721,045 B1).

Hunter discloses a method of manufacturing a semiconductor integrated circuit device performed in a semiconductor manufacturing apparatus having a plurality of chambers (col. 6, ll. 7-11), comprising the steps of obtaining an entire image (col. 21, ll. 62) of a semiconductor wafer after performing a first process to the semiconductor wafer in a first chamber of the plurality of chambers and before performing a second process to the semiconductor wafer in a second chamber of the plurality of chambers; determining the condition of the semiconductor wafer by examining the entire image of the semiconductor wafer; transporting the semiconductor wafer to the second chamber and performing the second process to the semiconductor wafer when the semiconductor wafer is determined to be in the proper condition; and stopping operation of the semiconductor manufacturing apparatus when the semiconductor wafer is determined to be in improper condition.

Hunter et al. further discloses that the first process includes one of a heat treatment method, a physical deposition method, a chemical deposition method, and a dry etching (col. 5, ll. 50-55).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter in view of Farber et al..

Hunter discloses a method of manufacturing a semiconductor integrated circuit device performed in a semiconductor manufacturing apparatus having a plurality of chambers (col. 6, ll. 7-11), comprising the steps of obtaining an entire image (col. 21, ll. 62) of a semiconductor wafer after performing a first process to the semiconductor wafer in a first chamber of the plurality of chambers and before performing a second process to the semiconductor wafer in a second chamber of the plurality of chambers; determining the condition of the semiconductor wafer by examining the entire image of the semiconductor wafer; transporting the semiconductor wafer to the second chamber and performing the second process to the semiconductor wafer when the semiconductor wafer is determined to be in the proper condition; and stopping

operation of the semiconductor manufacturing apparatus when the semiconductor wafer is determined to be in improper condition.

Hunter et al. further discloses that the first process includes one of a heat treatment method, a physical deposition method, a chemical deposition method, and a dry etching (col. 5, ll. 50-55).

Hunter et al. discloses the claimed invention with the exception of determining the condition of the semiconductor wafer by comparing the image of the semiconductor wafer and the image of a good semiconductor wafer taken in advance.

Farber et al. discloses a method of manufacturing a semiconductor integrated circuit device performed in a semiconductor manufacturing apparatus having a plurality of chambers (col. 10, ll. 55-67), wherein the method comprises obtaining a flat entire image of a semiconductor wafer after performing a first process to the semiconductor wafer in a first chamber and before performing a second process to the semiconductor wafer in a second chamber; determining the condition of the semiconductor wafer by examining the flat entire image of the semiconductor wafer (col. 4, ll. 39-51) by comparing a flat entire image of a good semiconductor wafer recorded in advance and the flat entire image of the semiconductor wafer; and making adjustment depending on whether the semiconductor wafer is found to be in proper or improper condition, wherein the examining of the flat entire image of the semiconductor wafer and using the information to determine the condition of the wafer between process steps is for the disclosed intended purpose of monitoring performance

of processing steps in a manner that require less manual interaction, produces more accurate results, and which can be performed in a fast and efficient manner such that more frequent monitoring can be performed in a cost effective manner.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Hunter et al. to include the image of a wafer determined to be in good condition in order to compare the image of the semiconductor wafer that is being worked on as Farber et al. teaches as both Hunter et al. and Farber et al. are directed to improving the discrimination process by which semiconductor wafers are selected for further process steps. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to compare the images as Hunter et al. discloses that the data obtained by the cameras is compared to information that is saved in the processing system.

Response to Arguments

5. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571)272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

Wael Fahmy
SPE 2814